Advanced Delay Analysis Method For Submicron ASIC Technology

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Abstract

This paper presents a new ASIC delay analysis method, in which two-dimensional delay table model is used for cells and the tailored circuit simulation is used for wires. Two factors of delay table are input waveform slope and load capacitance, which play most important roles for the variation of cell delay. In case of arbitrary RC tree load, we calculate the equivalent load capacitance by using node reduction technique and the proposed equation. This model preserves accurate delay estimation typically within 3% compared to that of HSPICE.

I. Introduction

The accurate delay modeling is essential for high-performance ASIC designs. As the size of transistor decreases continuously with the progress of semiconductor technology, the conventional linear delay model becomes inaccurate because it assumes the linearity of load capacitance dependent delay and constant input waveform slope [1]. Also, previous works [2,3] consider the wire RC loading, using a simple function and Penfield-Rubinstein technique [4]. But these techniques are applied under the several ideal conditions such as step input waveform. Therefore, for submicron technology which gate propagation delay no longer dominates over interconnect RC delay, these techniques become unreliable in delay estimation. In other works [5,6], the conventional circuit simulation was performed for the whole circuit after node reduction technique is applied. Though these techniques give more accurate results than the above, they require too much analysis time. Briefly, the former suffers from a lack of input waveform slope effect on wire delay, and the latter is impractical for VLSI design in execution time.

We propose a novel scheme which complements the demerits of previous approaches. After transforming the total wire parasitics into an equivalent load capacitance by the node reduction technique and proposed conversion equation, the propagation delay and output waveform slope of the cell on that load are calculated by the two-dimensional delay table model. Then, the tailored circuit simulation is applied to the wire part before the reduction. Finally, total path delay is calculated by summing cell delays and wire delays of paths connected from start node to end node.

In the next section, cell delay analysis method is explained and the path delay analysis method with RC parasitics is described in section 3. Section 4 and section 5 present experimental results and concluding remarks, respectively.

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II. Cell Delay Analysis

For the accurate analysis of cell delay, we should consider the major factors which affect the cell delay. They consist of input waveform slope, load capacitance, and derating factors such as temperature, voltage, and so on. Among these factors, the effects of the input waveform slope and load capacitance are more prominent than other factors. As shown Fig. 1, the variation of cell delay is not linearly proportional to any of two factors. Therefore, it becomes more and more difficult to derive a simple and accurate equation that reflects the input waveform slope and load capacitance effects. We solve these limitations by using a two-dimensional delay table model instead of equations. The table data including the propagation delay and output waveform slope for each cell are obtained by circuit simulation for several input waveform slopes and load capacitances. It takes a long time to generate the table data, but we can get necessary data quickly by using the automated process.

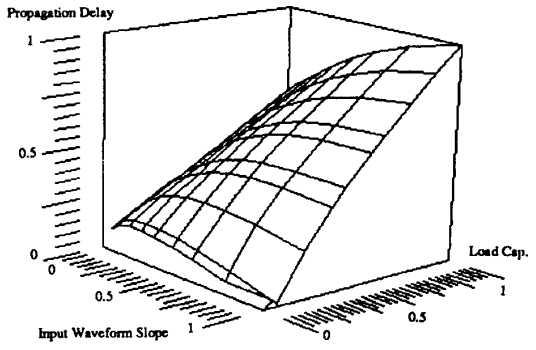

Fig. 1. Cell delay variation for the load capacitance and input waveform slope (normalized)

To explain the cell delay analysis method, a two-dimensional 4 x 4 plane graph is depicted on Fig. 2. Let's denote some factors as mathematical representations. $y_s[j][k]$ represents the propagation delay and the output

waveform slope of each cell, where j, $1 \le j \le m$, is a point on the input waveform slope axis and k, $1 \le k \le n$, is a point on the load capacitance axis. $x_{1a}[j]$ and $x_{2a}[k]$ represent the input waveform slope at point j and the load capacitance at point k. For example , it shows that m and n are 4 in Fig. 2. According to the above representations, $y_a[j][k]$ is a function of y which depends on $x_{1a}[j]$ and $x_{2a}[k]$.

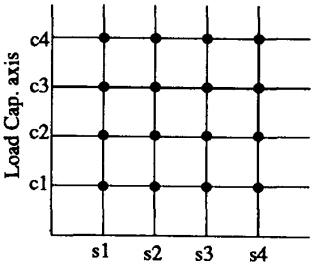

Fig. 2. 4x4 two dimensional plane graph

For any point (x_1, x_2), the propagation delay and the output waveform slope can be obtained by the following procedures.

1. Find the grid square which includes the point (x_1, x_2). The grid square is a part of two-dimensional planes. Fig. 3 shows the grid square which includes the point (x_1, x_2). Then, we can get j and k which satisfy the following conditions;

$$x_{1a}[j] \le x_1 \le x_{2a}[j+1] \quad (1)$$

$$x_{2a}[k] \le x_2 \le x_{2a}[k+1] \quad (2)$$

2. Extract the values of y_1, y_2, y_3, and y_4 from the table by using the following relationships;

$$y_1 \equiv y_a[j][k] \quad (3)$$

$$y_2 \equiv y_a[j+1][k] \quad (4)$$

$$y_3 \equiv y_a[j+1][k+1] \quad (5)$$

$$y_4 \equiv y_a[j][k+1] \quad (6)$$

3. Apply a bilinear interpolation method[7] as follows;

$$y(x_1, x_2) = (1 - t)\cdot(1 - u)\cdot y_1 + t\cdot(1 - u)\cdot y_2 + t\cdot u\cdot y_3 + (1 - t)\cdot u\cdot y_4 \quad (7)$$

where

$$t \equiv \frac{(x_1 - x_{1a}[j])}{(x_{1a}[j+1] - x_{1a}[j])} \quad (8)$$

$$u \equiv \frac{(x_2 - x_{2a}[k])}{(x_{2a}[k+1] - x_{2a}[k])} \quad (9)$$

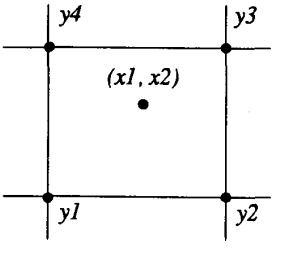

Fig. 3. An example of grid square

This procedure should be repeated twice. One is for the propagation delay, and the other is for the output waveform slope. If the appropriate grid square is not found in step 1, the most adjacent grid square should be selected, and then the extrapolation technique should be used.

III. Path Delay Analysis With RC Parasitics

To get the accurate result for path delay, it is important to estimate the RC loading effect on the driving cell and the interconnect delay. Using the node reduction technique and conversion equation, RC loading effect on the driving cell is substituted by the equivalent load capacitance. Then, this load capacitance is used in the two-dimensional table model. Also, the interconnection delay is estimated through the circuit simulation for the original RC tree.

The new conversion method of the equivalent load capacitance is divided into two phases. One is the node reduction phase [5] and the other is the conversion phase described below.

Node Reduction Phase

Let O denote the set of output nodes in the RC tree which are connected to the output of driving cell. And let C_{total} represent the sum of capacitances of the RC tree.

1. Calculate Elmore time constant for each output node of the given RC tree. Elmore time constant, T_{Di}, is represented by the following formula.

$$T_{Di} = \sum_{k=1}^{N} R_{ik}C_k \quad (10)$$

where

i: output node of RC tree.

k: node which is located between the source node and sink node.

N: number of nodes which are located between the source node and sink node.

R_{ik}: sum of resistance which are serially connected between the source node and node k.

C_k: capacitance value at node k.

2. Calculate R_{eq} and C_{eq} for each output node i, where R_{eq} and C_{eq} represent the equivalent resistance and equivalent load capacitance from start node to output node i, respectively.

$$C_{eq(i)} = \frac{C_i}{\sum_{k \in O} C_k} C_{total} \quad (11)$$

$$R_{eq(i)} = \frac{T_{Di(i)}}{C_{eq(i)}} \quad (12)$$

Conversion Phase

Let C and R denote the set of C_{eq}'s and R_{eq}'s obtained by node reduction phase.

1. Calculate R_{avg} and C_{sum}, where R_{avg} is the average value of the set R and C_{sum} is the total sum of set C.
2. To get the equivalent load capacitance of total wire parasitics, the following equation is used;

$$C_{load} = W_1 e^{W_2 R_{avg}} + W_3 C_{avg} + W_4 \quad (13)$$

where W_i's (i = 1, 2, 3, 4) are constant for each cell. The Fletcher-Powell technique [8] is used in determining W_i's which minimize the sum of the normalized squared errors between the equivalent load capacitance calculated by conventional circuit simulation and C_{load} calculated by Eq (13).

Fig. 4 shows an example circuit to explain this method and Fig. 5 shows the proposed transforming procedure.

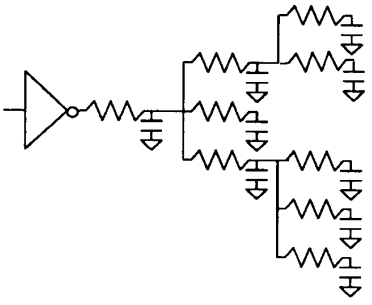

Fig. 4. An example circuit to explain the proposed model

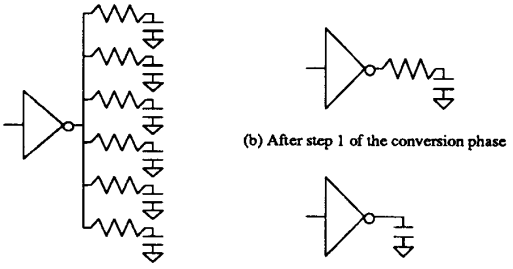

Fig. 5. The circuit structure transformed by the proposed scheme

IV. Experimental Results

To evaluate the accuracy and speed of the proposed model, we applied this model to several circuits which use our standard cell library. Test circuits were evaluated under 4 kinds of items.

1. Accuracy of delay estimation for each cell.
2. Accuracy of delay estimation for pre-layout paths.
3. Accuracy of delay estimation for post-layout paths.
4. Speed of delay estimation for pre- and post-layout paths.

Table 1 shows the cell characterization condition in constructing two-dimensional delay tables.

First, twenty-six cells are evaluated for several points and other delay models such as linear model, piecewise linear model and plane model (equivalent to 2 x 2 delay table model) are evaluated under the same condition to evaluate the accuracy of the proposed delay table model. Table 2 shows the test summary for the first item. The error percentages mean the average deviation between the delay estimation results by each model and the circuit simulation results. Compared to other models, the accuracy in the new method is improved from a minimal of 2.9 times to maximal of 6.0 times.

Simulation Condition	VDD = 4.5 V Temp. = 70 degree Process = Worst Case
Simulation Points	Input Waveform Slope(ns) : 0.1 1.0 3.0 5.0 Load Cap.(pf) : 0.06 0.3 3.0 6.0

Table 1. Conditions for cell characterization

Delay Model	Error Percentage(%)
Linear Model	4.27
PWL Model	3.74
Plane Model	2.04
Table Model	0.71

Table 2. The accuracy comparison of various delay models in cell delay estimation

Second, ten paths of the real circuit are evaluated. To observe the accuracy variation, as the cell characterization condition, delay tables are constructed under the five conditions which are shown in Table 3. Table 4 shows the accuracy comparison between the table model and the linear model.

CASE A	SLOPE	0. 1 2 5
	LOAD CAP.	0.05 0.3 1 2
CASE B	SLOPE	0.4 1.93 3.47 5
	LOAD CAP.	0.05 0.7 1.35 2
CASE C	SLOPE	0.4 3.6 6.8 10
	LOAD CAP.	0.05 1.37 2.68 4
CASE D	SLOPE	0.4 1.5 5
	LOAD CAP.	0.05 0.65 2
CASE E	SLOPE	0.4 0.8 1.3 2 5
	LOAD CAP.	0.05 0.2 0.4 1 2
CASE L	SLOPE	1.3
	LOAD CAP.	0.06 0.3

Table 3. Cell characterization conditions for the second item

As shown in Table 4, the results are 2.5 times more accurate, using the 4 x 4 delay table, than the 3 x 3 delay table. But the accuracy of 5 x 5 delay table does not supersede that of 4 x 4 delay table. From these facts, we found that the increase of characterization points of the delay table gives more accurate results, but when it reaches the reasonable number of points, the accuracy is not improved. Also, from case A and C in Table 4, it is known that the accuracy depends on the range of characterization points. Thus, characterization points should be chosen according to the fanout statistics of the given circuits. It is shown that the results of case L (linear model) do not produce better accuracy than those of other cases where the delay table model is used.